Electrical Properties of Epitaxial 3C- and 6H-SiC p-n Junction Diodes Produced Side-by-Side on 6H-SiC Substrates

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***Abstract*—3C-SiC (β-SiC) and 6H-SiC p-n junction diodes have been fabricated in regions of both 3C-SiC and 6H-SiC epitaxial layers which were grown side-by-side on low-tilt-angle 6H-SiC substrates via a chemical vapor deposition (CVD) process. Several runs of diodes exhibiting state-of-the-art electrical characteristics were produced, and performance characteristics were measured and compared as a function of doping, temperature, and polytype. The first 3C-SiC diodes which rectify to reverse voltages in excess of 300 V were characterized, representing a six-fold blocking voltage improvement over experimental 3C-SiC diodes produced by previous techniques. When placed under sufficient forward bias, the 3C-SiC diodes emit significantly bright green-yellow light while the 6H-SiC diodes emit in the blue-violet. The 6H-SiC p-n junction diodes represent the first reported high-quality 6H-SiC devices to be grown by CVD on very low-tilt-angle ($< 0.5^\circ$ off the (0001) silicon face) 6H substrates. The reverse leakage current of a 200 μm diameter circular device at 1100 V reverse bias was less than 20 nA at room temperature, and excellent rectification characteristics were demonstrated at the peak characterization temperature of 400°C.**

I. Introduction

In recent years there has been increasing interest and research on silicon carbide (SiC) as a wide-bandgap, high-breakdown field, high-thermal conductivity semiconductor for use in high-temperature, high-power, and/or high-radiation operating conditions under which silicon and conventional III-V semiconductors cannot adequately function. Its inherent material property advantages offer the possibility of improved electronics for a variety of applications such as hot-engine instrumentation and control (aerospace and automobile), power control, microwave radar and communications, and rad-hard circuits [1]–[13].

Silicon carbide occurs in many different crystal structures (called polytypes) with each crystal structure having its own unique electrical and optical properties. The two most commonly obtainable polytypes of SiC are 3C-SiC, a cubic structure with a 2.2 eV bandgap energy, and 6H-SiC, a hexagonal structure with a 2.9 eV bandgap. Techniques for growing 6H-SiC have advanced to the point where 1-in diameter wafers and high-quality epilayers are now commercially available [14]. This has lead to the fabrication of some extremely promising prototype 6H-SiC devices within the last few years [15]–[25].

3C-SiC has some material property advantages over 6H-SiC, such as higher low-field electron mobility, which might be exploited to produce superior devices and circuits for microwave power and other applications [26], [27]. Yet because no growth technique has been developed for obtaining semiconductor device quality single-crystal 3C-SiC on suitably large substrates, these property advantages have gone unrealized in experimental electrical devices. Given the lack of 3C-SiC substrates suitable for mass production, efforts have focused on heteroepitaxial growth of 3C-SiC layers on silicon and other potentially large-area, reproducible substrate materials. The crystallographic quality of the 3C-SiC resulting from previous efforts has been poor, containing unacceptably high densities of stacking faults, double-positioning boundaries (DPB's), microtwins, threading dislocations, and other undesirable crystal defects [28]–[30]. These defects manifest themselves in the poor electrical characteristics of diodes and transistors fabricated in the resulting 3C-SiC material. Prior to this work, 3C-SiC diode junctions at room temperature were very leaky, exhibiting large (mA/cm^2) current densities at less than 10 V reverse bias. The excessive current flow made 3C-SiC p-n junctions unsuitable for rectification purposes (in a diode or as a junction in a transistor structure) beyond a few tens of volts reverse bias [31]–[44]. As a result, the electrical characteristics of 3C-SiC transistors previously reported on substrates suitable for mass production have been extremely limited, and have failed to offer significant advantages over silicon-based technologies [41]–[49]. The only superior 3C-SiC devices reported to date were produced on as-grown Acheson furnace 6H-SiC crystals which are not generally considered suitable for mass production [50]–[52].

In 1991, Powell *et al.* reported on a technique for obtaining greatly improved quality 3C-SiC via chemical vapor deposition (CVD) growth on commercially available 6H-SiC wafers with low tilt-angles [53], [54]. The process, described briefly in the next section, yields a mixture of 1 mm^2 3C-SiC epilayer mesas and 1 mm^2 6H-SiC epilayer mesas on a single polished 6H-SiC wafer. In the regions that 3C-SiC is grown,

Manuscript received June 18, 1993; revised December 17, 1993. The review of this paper was arranged by Associate Editor T. P. Chow. This work was supported by the NASA Lewis Research Center.

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IEEE Log Number 9400610.

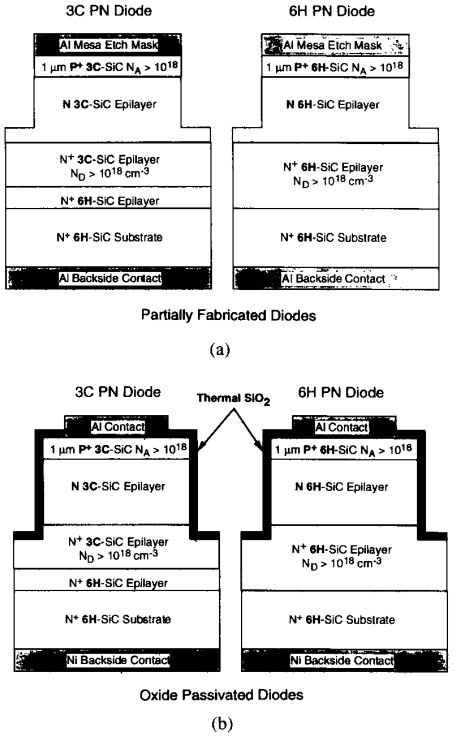


Fig. 1. Cross sections of (a) partially fabricated devices that were preliminarily characterized with most of the reactive ion etch process completed, and (b) the completely fabricated devices with wet thermal SiO_2 oxide passivation.

the technique has successfully eliminated all DPB defects on the majority of 1 mm^2 mesas, leaving reduced densities of stacking faults as the only observed crystallographic defects present in the resulting 3C-SiC epilayers. This paper reports on a set of experiments in which a series of epitaxial 3C- and 6H-SiC p-n junction diodes were fabricated side-by-side on the same wafer. The state-of-the-art electrical performance characteristics obtained from these diodes are presented as a function of doping, temperature, and polytype.

II. Experimental Procedures

The 3C-SiC and 6H-SiC epilayers shown schematically in Fig. 1 were grown on commercially available [14] 6H (0001) silicon-face SiC substrates with tilt angles ranging from 0.2° to 0.3° (where 0° = the [0001] SiC basal plane). Wafer tilt angles were measured using an x-ray/laser technique, but tilt direction was not correlated with crystal direction [55]. A series of equally spaced 50 μm deep grooves were cut into the growth surface of each wafer using a dicing saw, which defined an array of square 1 mm^2 mesas on each wafer. These wafers were used as substrates in subsequent CVD growth, which produced a mixture of 1 mm^2 3C-SiC epilayer mesas and 6H-SiC epilayer mesas on each SiC wafer [53], [54], [56]. To produce the 3C- and 6H-SiC epilayers, silane (3% in H_2) and propane (3% in H_2) were flowed into an atmospheric pressure CVD reactor using a carrier gas of ultra-purified hydrogen. These precursor gases subsequently

TABLE I
N-Type Active Layer Thickness and Measured Doping Parameters for SiC p-n Diodes

Sample	n Layer Thickness (μm)	3C n Layer Doping (cm^{-3})	6H n Layer Doping (cm^{-3})
1494-1	6	$1.3\text{-}2.1\times10^{18}$	$1.2\text{-}2.1\times10^{18}$
1495-1	6	$0.85\text{-}1.1\times10^{17}$	$1.1\text{-}1.3\times10^{17}$
1506-1	5	$0.5\text{-}2\times10^{16}$	$0.5\text{-}2\times10^{16}$
1511-4	24	$3\text{-}5\times10^{15}$	$3\text{-}5\times10^{15}$

pyrolyzed on the 6H-SiC substrates which were heated to 1450°C via an inductively heated, SiC-coated graphite susceptor. The positional distribution of 3C epilayer mesas versus 6H epilayer mesas on the wafer was random, and the percentage of 3C mesas was roughly 50%. During the CVD growth process, p-type epilayers were produced by the introduction of trimethylaluminum (via a bubbler configuration) whereas a flow of nitrogen (100 atomic ppm in H_2) was used for n-type epilayer formation. Four variations in doping and active epilayer thickness were grown and investigated in this experiment, as summarized in Table I. The active layer doping densities were obtained from C-V measurements on the finished p-n junction diodes. The lighter-doped samples 1506-1 and 1511-4 were produced using a new silicon carbide CVD growth technique, called site-competition epitaxy, developed by Larkin *et al.* [56], [57]. The 3C/6H heterojunctions were buried in heavily doped n^+ material in order to minimize any heterojunction parasitic effects which might interfere with the measurement of 3C-SiC homodiode electrical properties. Preliminary characterization of significantly improved oxide-passivated 3C-SiC diodes from sample 1506-1 was initially reported in [58] and [59], and brief results from 6H and 3C diodes on samples 1506-1 and 1511-4 were previously presented in [18] and [56].

Processing of all four samples was done in parallel, with pattern definitions, metallizations, etches, and oxidations being done simultaneously. To begin the post-growth diode fabrication, a 2000 Å thick aluminum etch mask, which defined circular and square diode mesas ranging in area from 7×10^{-6} cm^2 to 4×10^{-4} cm^2, was applied and patterned by metal liftoff. The diode mesas were etched to a depth of approximately 6 μm using reactive ion etching (RIE) with 80% SF_6: 20% O_2 at 300 W rf with a chamber pressure of 250 mTorr. Immediately following the mesa definition etch, aluminum was E-beam evaporated onto the backside of the wafers, resulting in the device cross-sections shown in Fig. 1(a). At this stage in the fabrication process, some devices on all the wafers were probe tested at room temperature. The measurements taken during this mid-processing electrical testing are presented in Section III. Sample 1511-4 did not undergo any further processing.

Following the brief electrical measurements without oxide passivation, the samples (except 1511-4) were returned to the RIE for an additional 2 μm of etching to ensure that the mesa etch extended into the heavily-doped n-type epilayer. The aluminum etch mask and backside contact were stripped

by wet etch, and then a cleanup dip in boiling sulfuric acid was performed. The samples underwent wet thermal oxidation for 6 hours at 1150°C to form SiO_2 at least 500 Å thick [60]. After the wafers had been patterned for topside contacts, vias were etched in the oxide using 6:1 buffered HF solution. Aluminum was E-beam deposited and lifted off to form the topside contacts, and unpatterned nickel was sputtered onto the backside to complete fabrication of the device cross sections shown in Fig. 1(b). No contact anneals were performed in this work for the simple reason that the measurement of fundamental rectification properties could be accomplished without minimizing contact resistances. Current-voltage measurements were carried out in the dark using computer controlled source-measurement units, and current versus voltage (I-V) plots were generated from the resulting digital data.

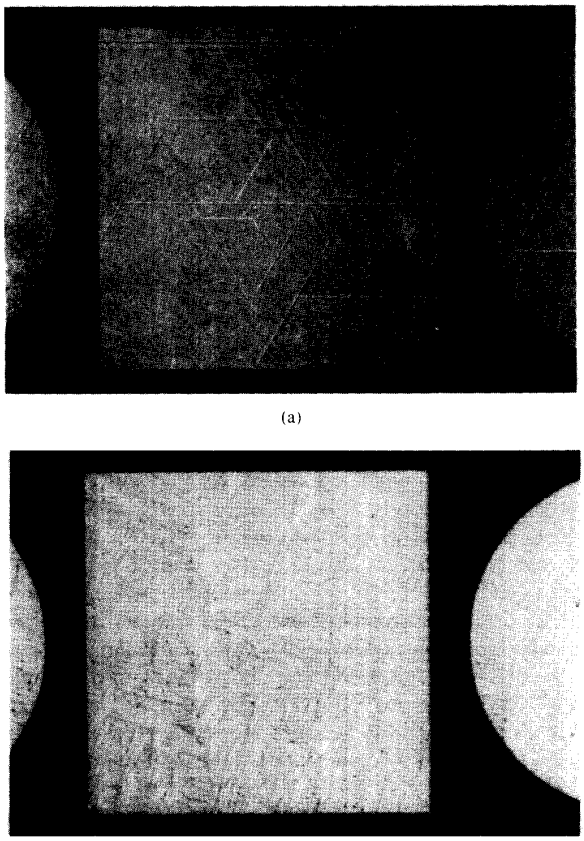
III. Results

A. General

Although the growth technique produces regions of both 3C and 6H epilayers on any given wafer, identification of each device's polytype on the oxidized wafers was facilitated by the different oxidation rates of the 3C and 6H polytypes [61]. The observed oxide color difference resulting from the thicker 3C oxide clearly distinguished 3C devices from 6H devices on each wafer [60], [61]. Furthermore, the oxidation also delineated stacking faults and double positioning boundaries (DPB's) present in the 3C regions of each wafer [61]. Most 3C mesas were free of DPB's. The few 3C diodes that did have DPB's running through them did not exhibit appreciable rectification compared to the rectification observed on DPB-free 3C diodes. The stacking fault densities varied from mesa to mesa, but the density was significant enough that almost every 3C device measured in this work contained at least one stacking fault. A photograph of the stacking faults present (visible in as lines) in an oxidized 3C-SiC diode mesa prior to contact via etching and metallization is shown in Fig. 2(a). Most 6H mesa device areas were free of observed crystal defects as documented by the photograph of Fig. 2(b). For unkown reasons, the second etch processing step introduced shallow texture and poc marks that are visible in Fig. 2.

When placed under sufficient forward bias, the 3C diodes emitted light that was visually observed to range in color from yellow to green, while diodes in the 6H-regions emitted light visually ranging from blue to violet (Fig. 3). To the best of the authors' knowledge, the green-yellow light seen in Fig. 3 represents the first report of significantly bright green-yellow light emission from a CVD-grown 3C-SiC diode.

Capacitance-voltage (C-V) measurements on the larger-area 3C and 6H diodes were used to ascertain the carrier concentration of each sample's lighter-doped layers. The range of apparent carrier concentration values obtained is listed in Table I. Plots of $1/C^2$ versus V were linear, reflecting the abrupt step-like nature of the junctions, and the x-intercepts obtained on the 6H devices were larger, reflecting the built-in voltage difference between 3C and 6H polytypes arising from the larger 6H bandgap. The current-voltage (I-V) characteristics of



(a)

(b)

Fig. 2. Oxidized 200 μm × 200 μm (a) 3C-SiC and (b) 6H-SiC diode mesas on the same 6H-SiC wafer prior to contact metallization. There were significant variations in the number of stacking faults, visible as the "line segments" running through the device of part (a), present on each 3C mesa. The vast majority of 6H diode mesas exhibited no observed crystal defects.

the 3C diodes were significantly different from the 6H diode characteristics. In all cases, there was a consistent correlation between the color of light emitted by a diode under forward bias, its measured electrical characteristics (i.e., a "3C-like" I-V and C-V characteristic versus a "6H-like" I-V and C-V characteristic), and its polytype as identified by observing the device oxide color.

B. 3C-SiC Diode Characteristics

Representative linear-scale current-voltage characteristics obtained from the 3C p-n junction diodes at room temperature are displayed in Fig. 4. The dashed-line curves represent I-V characteristics taken with unpassivated device sidewalls (Fig. 1(a) device configuration), while the solid-line curves were taken from completed devices with wet-thermal-oxide sidewall passivation (Fig. 1(b) device configuration). The reverse and forward characteristics of the 3C p-n junction diodes are re-plotted separately in a semi-logarithmic fashion in Figs. 5 and 6. In every case the reverse breakdown characteristics degraded during the final device fabrication steps. The actual cause of this degradation is not known at this time. Consistent with the fact that the number of stacking faults varied from

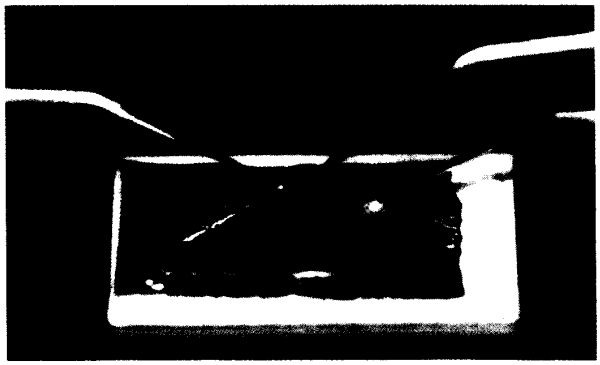


Fig. 3. Blue-violet 6H-SiC and green-yellow 3C-SiC light emitting diodes fabricated from epilayers grown by CVD on the same low-tilt-angle 6H-SiC wafer. Almost all the p-n junction diodes produced in this work exhibited significantly bright light emission similar to what is shown in this photograph.

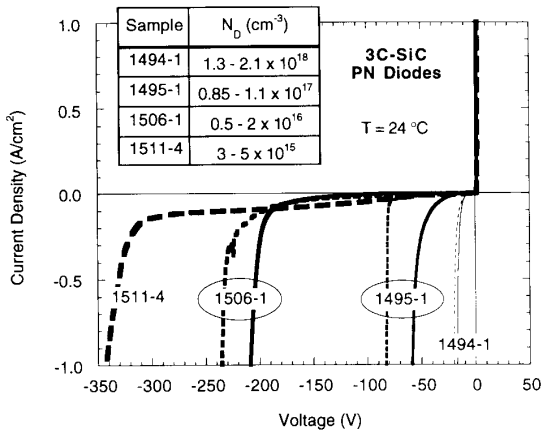


Fig. 4. Linear scale current-voltage characteristics taken from representative epitaxial 3C-SiC p-n junction diodes at room temperature. The dashed lines indicate measurements taken from the partially fabricated devices (Fig. 1(a) cross section), while the solid lines indicate the measured characteristics of oxide passivated devices (Fig. 1(b) cross section).

device to device, there were some notable variations in reverse leakage characteristics measured among 3C devices on the same wafer, even among same-sized 3C diodes within the same 1 mm × 1 mm saw-cut mesa. Nevertheless, greater than half of all 3C-SiC diodes tested in this work exhibited effective blocking voltages within 20% of those depicted in Fig. 4.

Prior to this work, no 3C-SiC p-n junction diode had demonstrated rectification to voltages beyond 50 V reverse bias. Also, there had not been any reported experimental observations of avalanche breakdown in a 3C-SiC p—n junction diode. The 300 V blocking voltage of the 1511-4 3C diodes represents a six-fold improvement in 3C-SiC p-n junction diode blocking voltage reported prior to this work [31]–[44]. The vastly improved diode characteristics are directly attributable to recent improvements in the 3C-SiC CVD growth process which have increased crystal purity, eliminated DPB defects, and greatly reduced stacking fault densities [53], [54], [56], [57]. However, the breakdown characteristics of 3C diodes on samples 1506-1 (with and without sidewall oxide passivation) and 1511-4 were soft in nature, and are not attributed to bulk breakdown. The soft breakdown was repeatable (i.e.,

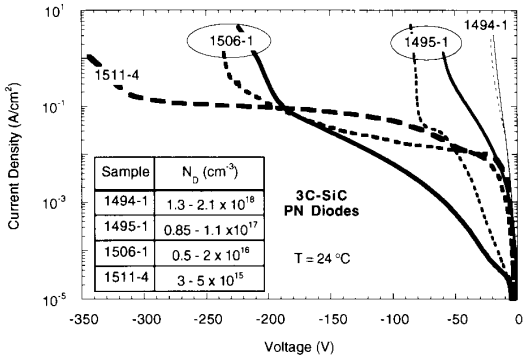


Fig. 5. Semi-logarithmic plot of reverse current-voltage characteristics of epitaxial 3C-SiC p-n junction diodes at room temperature. The dashed lines indicate measurements taken from the partially fabricated devices (Fig. 1(a) cross section), while the solid lines indicate the measured characteristics of oxide passivated devices (Fig. 1(b) cross section).

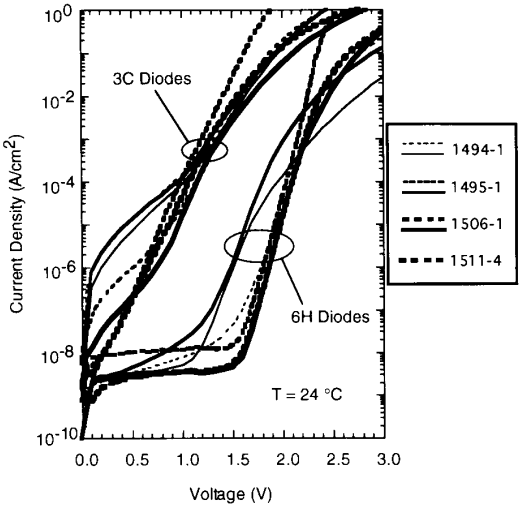


Fig. 6. Semi-logarithmic plot of forward-biased current-voltages characteristics measured on epitaxial 3C- and 6H-SiC p-n junction diodes at room temperature. The dashed lines indicate measurements taken from the partially fabricated devices (Fig. 1(a) cross section), while the solid lines indicate the measured characteristics of oxide passivated devices (Fig. 1(b) cross section). The 6H diodes exhibited consistent forward exponential ideality factors near 2.

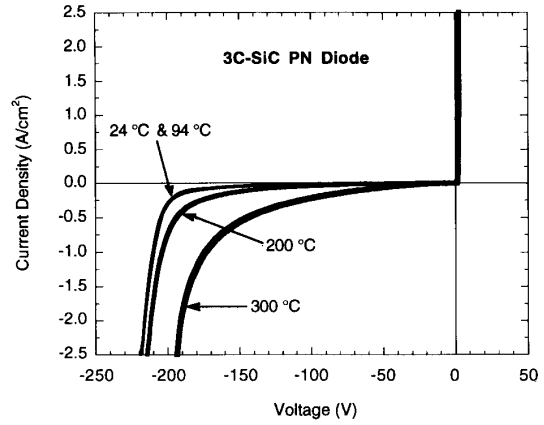
the curve can be taken numerous times with no change in device characteristics) only when the current flowing during reverse breakdown is restricted to less than one milliamp; unlimited current flow results in permanent damage to the diode. In the oxide-passivated sample 1506-1, coronas of microplasmas [62]–[65] were observed exclusively around device boundaries during breakdown suggesting that reverse failures are occurring at the mesa perimeter and are not due to a bulk mechanism. Once a particular diode had been catastrophically damaged by excessive current flow during breakdown, the multi-microplasma corona was replaced by a single microplasma which presumably was the point of catastrophic device failure along the mesa edge sidewall.

Unlike their lightly-doped counterparts, the heavier-doped 3C-SiC diodes on samples 1494-1 and 1495-1 exhibited bulk junction breakdown characteristics. The 3C devices measured

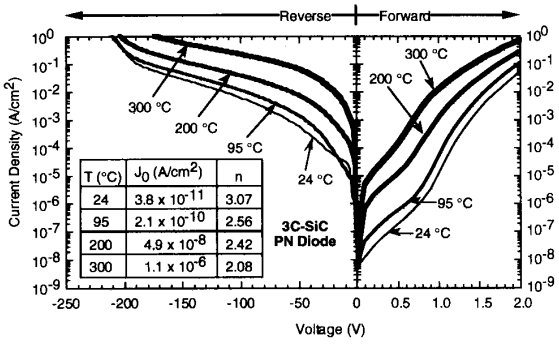
on sample 1495-1 prior to sidewall oxide passivation exhibited a sharp, repeatable increase in reverse current consistent with typical avalanche breakdown characteristics [65]–[67] (Figs. 5 and 13). It is our belief that the data of Figs. 5 and 13 may represent the first reported electrical observation of avalanche breakdown in a 3C-SiC p-n junction diode. Unfortunately, the temperature dependence of the breakdown voltage could not be measured for this device, because of the unexpected degradation in the rectifying characteristics of the diodes following sidewall-oxide-passivation. Sharp breakdown was not observed in the 3C diodes of 1494-1, but this is because carrier tunnelling should be the dominant leakage mechanism at the 1-2 $\times$ 10^{18} cm^{-3} doping levels present in the 2.2 eV bandgap 3C-SiC p-n diode sample [66]. In addition to coronas of microplasmas observed around the mesa peripheries of the sidewall-passivated 1494-1 and 1495-1 3C diodes, microplasmas were also clearly visible in the bulk mesa regions not obscured by the metal contact. These devices were far less susceptible to excessive reverse current flow, as repeatable breakdown characteristics were obtained in most devices without restricting reverse current during measurements.

Fig. 7 details the forward and reverse I-V characteristics of a representative sidewall-passivated 3C diode from sample 1506-1 at elevated temperatures. Although determination of a quantitative improvement factor naturally depends upon the voltage and temperature selected as a basis of comparison, the 1506-1 3C-SiC diodes clearly represent at least an order of magnitude reduction in reverse leakage current density compared to all 3C-SiC p-n diodes published prior to this work [31]–[44]. The exponential regions of the forward-bias characteristics exhibit record low saturation current densities for CVD-grown 3C p-n diodes [31]–[39], [42]–[44]. However, the change in ideality factors with temperature is not well understood at this time. As confirmed by measurements on contact test structures, the nonexponential behavior limiting the forward current at larger forward biases in Figs. 6 and 7(b) is due to the parasitic reverse-biased Schottky barrier formed between the unannealed top aluminum contact and the p^+ cap layer.

Thermal activation energy plots of the reverse currents did not yield linear Arrhenius-like results, and the reverse current was not proportional to the square root of the applied voltage. These facts, coupled with the fact that the current density was excessive compared to generation currents observed in narrower-bandgap semiconductor p-n junctions, suggest that mechanisms other than thermal generation were responsible for the 3C reverse leakages. Surmising that the stacking fault defects were the primary source of 3C diode leakage, an attempt was made to quantitatively correlate the measured reverse currents with observable stacking fault parameters on the oxidized samples. However, no correlation between stacking fault defect parameters (e.g., the number of faults in the device mesa, the apparent fault length within each mesa, the number of stacking fault/stacking fault intersections, and the number of stacking fault intersections with the mesa periphery) and the measured reverse leakage current densities in the 3C diodes was conclusively established.



(a)



(b)

Fig. 7. The current-voltage characteristics taken at several temperatures from an oxide passivated (Fig. 1(b) cross section) 100 μm $\times$ 100 μm epitaxial 3C-SiC diode on NASA Sample 1506-1. (a) Linear scale plot, and (b) semi-logarithmic plot. The ideality factors (n's) and saturation current densities (J_0's) of the exponential forward regions of the I-V's are given in the inset of part (b).

C. 6H-SiC Diode Characteristics

As one would expect from the absence of stacking faults and other observed crystal defects in most of the epitaxial 6H-SiC devices, the 6H-SiC p-n junction diodes exhibited superior, more consistent electrical characteristics than the 3C-SiC diodes. Fig. 8 shows representative linear-scale current-voltage characteristics obtained from the 6H-SiC p-n junction diodes at room temperature. Again, the dashed-line characteristics represent I-V's taken with unpassivated device sidewalls (Fig. 1(a) device configuration), while the solid-line curves represent characteristics taken from completely fabricated devices with wet thermal oxide sidewall passivation (Fig. 1(b) device configuration). The forward and reverse characteristics of Fig. 8 are replotted separately in a semi-logarithmic fashion in Figs. 6 and 9.

Sharp, avalanche-like breakdown was not observed in the lightly doped high-voltage 6H-SiC p-n diodes. Despite the use of Fluorinert^{TM} (a high dielectric strength insulating fluid [68]) to minimize surface arcing, catastrophic reverse failures repeatedly occurred between -600 and -700 V on the 6H diodes on sample 1506-1. Lightning-bolt like electrical

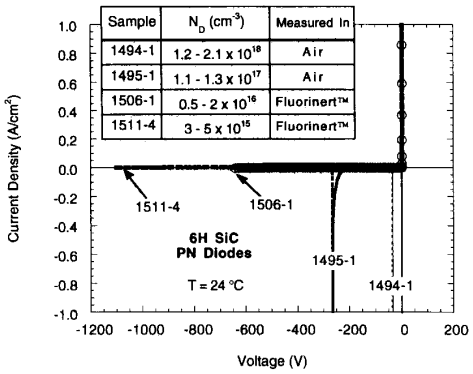


Fig. 8. Linear scale current-voltage characteristics taken from representative epitaxial 6H-SiC p-n junction diodes at room temperature. The dashed lines indicate measurements taken from the partially fabricated devices (Fig. 1(a) cross section), while the solid lines indicate the measured characteristics of oxide passivated devices (Fig. 1(b) cross section). The low-voltage samples were probed in air, while the high-voltage samples were measured immersed in Fluorinert™ to minimize high-voltage arcing.

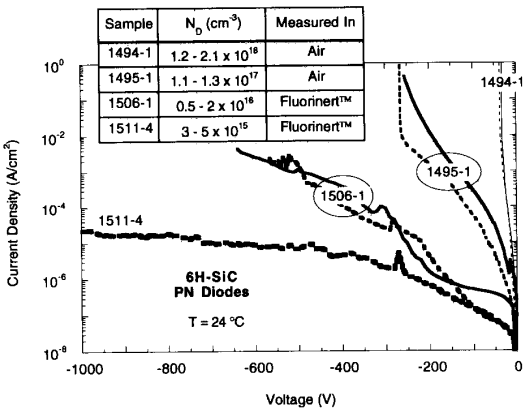
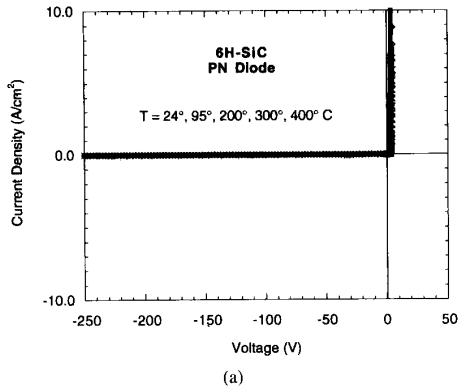
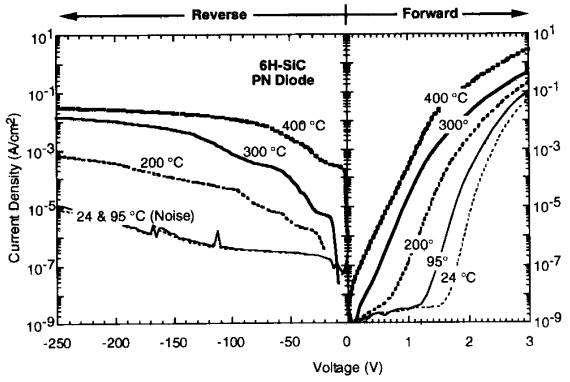


Fig. 9. Semi-logarithmic plot of reverse current-voltage characteristics of epitaxial 6H-SiC p-n junction diodes at room temperature. The dashed lines indicate measurements taken from the partially fabricated devices (Fig. 1(a) cross section), while the solid lines indicate the measured characteristics of oxide passivated devices (Fig. 1(b) cross section). The low-voltage samples were probed in air, while the high-voltage samples were measured immersed in Fluorinert™ to minimize high-voltage arcing.

arcs (not microplasmas) were observed when the 1506-1 devices failed during high-voltage testing, suggesting that localized failure was occurring along nonoptimized high-field surface regions of the diodes and not taking place within the semiconductor. The breakdown voltage of sample 1511-4, which had no sidewall passivation, exceeded the laboratory equipment's maximum operating voltage of −1100 V when immersed in Fluorinert™. At −1100 V applied bias, a room-temperature leakage current of less than 20 nA was recorded on the 200 μm diameter diode whose reverse current density versus voltage data is shown in Figs. 8 and 9. The higher-doped 6H diodes from samples 1494-1 and 1495-1 exhibited reverse breakdown characteristics at voltages consistent with those previously reported in the literature for 6H-SiC pn junction diodes [15]–[17]. Both bulk and perimeter microplasmas were visible in the oxidized breakdown-biased 6H diodes from 1494-1 and 1495-1.



(a)



(b)

Fig. 10. The current-voltage characteristics of an oxide-passivated (Fig. 1(b) cross section) 200 μm diameter epitaxial 6H-SiC diode on NASA Sample 1506-1 at temperatures ranging from 24°C to 400°C. (a) Linear scale plot and (b) semi-logarithmic plot. Fig. 10(a) demonstrates the excellent diode rectification maintained at all temperatures in this work, as the differences between the I-V curves were negligible on the linear scale.

The forward and reverse I-V characteristics taken at several temperatures from a representative 200 μm diameter 6H-SiC diode on sample 1506-1 with sidewall oxide are presented in Fig. 10. The linear-scale I-V curves plotted in Fig. 10(a) illustrate the excellent rectification properties that the 6H-SiC diodes maintained over the range of temperatures (24° C–400°C) investigated in this work. The temperature dependence is more clearly shown in the semi-logarithmic plot of the same I-V curves in Fig. 10(b). It should be noted that the reverse-bias curves at 24° and 95° C were actually the background noise of the measurement apparatus, since the same curve resulted when the probes were open-circuited above the diode. Because the use of Fluorinert™ was impractical above room temperature, the maximum applied reverse voltage was restricted to −250 V to avoid the possibility of arcing damage to the device.

The measured 6H-SiC diode I-V characteristics exhibited much less scatter than their 3C counterparts. Within that context, it should be noted that sample-to-sample variation observed among the measured 6H reverse leakage currents was larger than the scatter observed in the measured forward characteristics of the 6H diodes. This is presumably due to the fact that point and/or line defects (located either in the sidewall

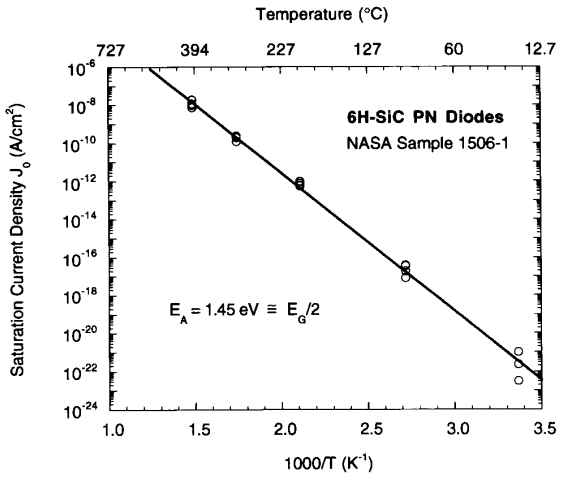


Fig. 11. Activation energy plot showing the temperature performance of the exponential forward saturation current density (J_0) for completed (Fig. 1(b) cross section) 6H-SiC diodes on NASA Sample 1506-1. The near half-bandgap activation energy suggests that the centers dominating the forward recombination current reside energetically near the middle of the bandgap.

oxide or the bulk crystal) are generally more detrimental to the reverse I-V characteristics, where the magnitudes of ideal currents are smaller and applied voltages are larger, than to the forward I-V characteristics.

Representative measured room-temperature forward I-V characteristics from all the 6H-SiC p-n junction diode samples are plotted semi-logarithmically in Fig. 6. Unlike their 3C-SiC counterparts (also shown in Fig. 6), the 6H diodes consistently exhibited forward exponential saturation current ideality factors (n factors) very close to 2 at room temperature. This suggests that the dominant forward conduction mechanism is recombination of carriers at defect centers within the space-charge region, as opposed to diffusion which would yield ideality factors closer to unity [65], [66], [69], [70]. Using the common assumption that the dominant recombination centers reside energetically near the middle of the bandgap, the temperature dependence of the recombination current is dominated by the intrinsic carrier concentration n_i, whose exponential temperature dependence yields a thermal activation energy of close to half the semiconductor band gap [66], [69]–[73]. The temperature dependence of the forward saturation current density (J_0) of 6H-SiC diodes from 1506-1 is shown in the Arrhenius plot of Fig. 11. The observed thermal activation energy of 1.45 eV is essentially half the 6H-SiC bandgap (E_G = 2.9 eV for 6H-SiC).

IV. Discussion

As one would expect from the higher crystalline quality of the epitaxial 6H-SiC relative to the epitaxial 3C-SiC, the 6H-SiC p-n junction diodes exhibited superior, more consistent electrical characteristics than the 3C-SiC diodes. Though much new information has been documented in this work, the experimental data raises an assortment of new questions that remain to be addressed. Chief among these are sorting out the electrical effects of the sidewall oxidation process (on both 3C and 6H diodes) and the role of the stacking faults that remain in the 3C material. As can be seen from the data presented in Figs. 4–6, 8, and 9, there were significant differences between the partially fabricated (Fig. 1(a) cross section) and completely fabricated (Fig. 1(b) cross section) diode I-V characteristics. The causes of these differences, which arose to varying degrees in both polytypes, is unclear at this time. C-V measurements of metal-oxide-semiconductor capacitor (MOS-C) devices oxidized in the same system that produced the diode sidewall oxides have suggested that serious furnace contamination problems existed when these devices were fabricated [74]. However, the degree to which the contamination might be affecting the electrical properties of the sidewall oxides and its resulting affects on diode current-voltage characteristics was not ascertained in this work.

Despite the aforementioned problems, the vast improvement in 3C-SiC crystalline quality has nevertheless unlocked some fundamental electrical properties that had not been previously documented at an experimental level. One such property of great significance is the experimental breakdown field of 3C-SiC. The maximum electric field present in a one-sided step diode junction at breakdown (E_m, the breakdown field) is given by [66], [67]:

$$E_m = \sqrt{\frac{2qN_B V_{\rm br}}{\varepsilon_S}} \tag{1}$$

where N_B is the doping on the lighter-doped semiconductor side of the junction, ε_S is the semiconductor dielectric constant and $V_{\rm br}$ is the reverse voltage at which breakdown occurs in the diode. Fig. 12 shows the breakdown fields calculated by applying (1) to the apparent breakdown voltages measured in this work. Prior experience with silicon p-n junctions suggests that the presence of bulk breakdown microplasmas observed in the SiC devices should not have significantly lowered the measured breakdown voltages below the bulk microplasma-free avalanche breakdown value [62], [63]. The error bars in Fig. 12 represent the range of values calculated from the minimum and maximum combinations of the measured doping (Table I) N_B and the measured breakdown voltage $V_{\rm br}$. Though sharp breakdown was not observed in the 3C diodes from sample 1494-1, it is nevertheless reasonable to calculate a minimum value for the breakdown field based on the minimum reverse blocking voltages observed. Samples 1506-1 and 1511-4 are omitted because softer, edge-microplasma-dominated breakdown was observed in these lighter-doped specimens. As depicted in Fig. 12, the 6H-SiC breakdown fields obtained in this work agree well with prior reported work on 6H-SiC diodes. Though the 3C-SiC breakdown fields are less than measured 6H-SiC breakdown fields, the 3C-SiC nevertheless exhibits a substantial (about a factor of three) breakdown field advantage over silicon, and is well above the 6×10^5 V/cm predicted by Tsukioka *et al.* via Monte Carlo simulations [75].

In addition to the differences in breakdown field, there are other obvious electrical disparities between the 3C and 6H diodes produced in this work. The material inequalities observed in this work are perhaps best illustrated by Fig. 13, which directly compares the reverse I-V characteristics of unpassivated 3C and 6H diodes from sample 1495-1 on

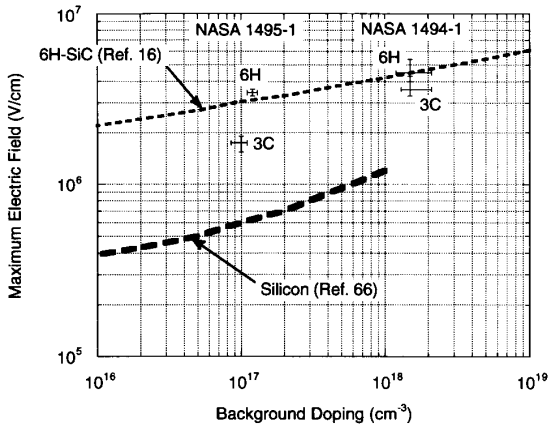


Fig. 12. Breakdown fields calculated from the 3C and 6H p-n diode breakdown voltages measured in this work compared with previously published silicon and 6H-SiC breakdown fields. The error bars represent the range of values calculated from the minimum and maximum combinations of the measured doping N_B and the measured breakdown voltage $V_{\rm br}$.

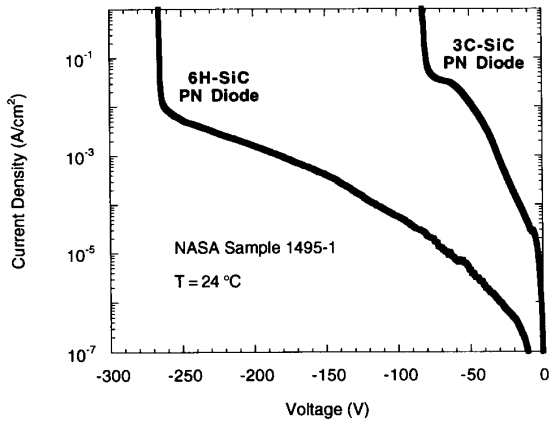


Fig. 13. Semi-logarithmic plot comparing the reverse I-V characteristics 3C- and 6H-SiC epitaxial p-n diodes from NASA Sample 1495-1. Both diodes were 200 μm diameter circular devices and both were measured prior to oxide passivation (Fig. 1(a) cross section).

a logarithmic current scale. These devices were chosen for illustrative comparison because they were identical in geometry (200 μm diameter circular mesas), both exhibited sharp, avalanche-like breakdown, and both were measured prior to the unexpected I-V degradation following oxidation. Even though clear experimental correlation was not obtained in this work, it is our opinion that the stacking faults present in the 3C diodes were responsible for the majority of the differences between 3C and 6H reverse leakages, forward saturation currents, and forward ideality factors. We are hopeful that the elimination of stacking fault defects in future 3C epitaxial material will be possible, and that this will lead to further substantial improvements in 3C-SiC diode performance.

V. Summary

In summary, 3C- and 6H-SiC p-n junction diodes have been epitaxially grown and fabricated side-by-side on the same commercially available 6H-SiC substrates. The record-setting 3C diodes demonstrated the first reported 3C-SiC rectification to 300 volts (a six-fold improvement over 3C-SiC diode blocking voltages fabricated by prior techniques), and the first report of significantly bright CVD-grown 3C-SiC light emitting diodes. For the first time, sharp reverse breakdown characteristics have been observed in a 3C-SiC p-n junction diode. The vastly improved diode characteristics are directly attributable to improvements in the 3C-SiC CVD growth process which have increased crystal purity, eliminated double-positioning-boundary (DPB) defects, and greatly reduced stacking fault densities. These results should lead to substantial advancements in the capabilities and performance of most single-crystal 3C-SiC electrical devices. However, there is still room for improvement in the 3C epitaxial material quality and electrical device characteristics, as some stacking faults are still present in the 3C-SiC epilayers and diodes.

The 6H-SiC p-n junction diodes produced represent the first report of high-quality 6H-SiC devices to be grown by CVD on 6H-SiC substrates with tilt angles of less than half a degree. The reverse leakage current of a 200 μm diameter circular 6H-SiC device at 1100 V reverse bias was less than 20 nA at room temperature, and excellent rectification characteristics were demonstrated at the peak measurement temperature of 400°C. The 6H-SiC diodes outperformed the 3C-SiC diodes, but this is primarily because 6H-SiC homoepitaxial growth on 6H substrates is further-advanced than 3C-SiC heteroepitaxial growth on 6H substrates. In addition to paving the way for greatly improved 3C-SiC transistors and circuits, these results open the possibility of incorporating both 3C- and 6H-SiC devices onto a single-chip for hybrid integrated circuit and optoelectronic applications.

Acknowledgment

The authors would like to acknowledge Jeremy B. Petit for his contributions to this work.

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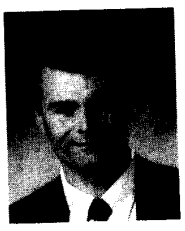
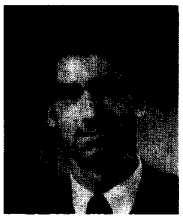


Philip G. Neudeck (S'87–M'92) received the B.S.E.E. (honors), M.S.E.E. and Ph.D. degrees from Purdue University, West Lafayette, IN, in 1986, 1987, and 1991, respectively.

In 1991 he joined the High Temperature Integrated Electronics and Sensors (HTIES) group at NASA Lewis Research Center in Cleveland, OH. He is currently researching the development of silicon carbide semiconductor electronics for use in high-temperature, high-power, and/or high-radiation applications.



David J. Larkin received the B.S. degree in chemistry and mathematics from the State University College at Oneonta in 1986 and the Ph.D. in inorganic chemistry from Rensselaer Polytechnic Institue in 1991.

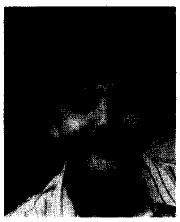
He joined NASA Lewis Research Center in 1991, where he has been involved in silicon carbide research for high temperature semiconductor applications. His other research interests include the development of organometallic precursors as low temperature, low pressure CVD routes to epitaxial silicon carbide.

Jonathan Starr received the B.S. degree in electrical engineering from the University of Massachusetts in 1992, and is now studying for the M.S. degree at the University of California at Santa Barbara. During the summers of 1992 and 1993 he assisted the High Temperature Integrated Electronics and Sensors research group at NASA's Lewis Research Center with research on the properties of epitaxial layers and microelectronic device structures made with 4H, 6H, and 3C silicon carbide.

J. Anthony Powell (M'77) received the B.S.E.E. in 1959 and the M.S. in physics in 1963, both from the University of Kentucky.

He joined NASA Lewis Research Center in 1963, where he is now a Senior Research Physicist. He has spent the majority of time at NASA pioneering silicon carbide (SiC) as a practical semiconductor material. In particular, he has developed new chemical vapor deposition (CVD) processes for growth of various SiC polytypes.

Mr. Powell is a member of the American Physical Society.



Carl Salupo is currently a Senior Electronic Technician working for Arvin/Calspan at NASA Lewis Research Center, where he works on silicon carbide process development and device fabrication. He has worked in semiconductor and thin film process development since 1979, and has coauthored several technical papers. Before joining NASA, he was employed by the BP America Research Center and Case Western Reserve University.

Lawrence G. Matus received the B.A. degree (honors) in chemistry from Oberlin College, Oberlin, OH in 1978 and the Ph.D. degree in analytical chemistry from North Carolina State University, Raleigh, NC, in 1983.

He joined NASA Lewis Research Center in 1983, where he has been working in the Engine Sensor Technology Branch. He has been researching silicon carbide as a high temperature semiconductor material. His present research interests as a Senior Research Scientist include silicon carbide as a material for microelectromechanical systems (MEMS) applications.